Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte JAY D. JETER and RONALD J. LANDRY

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Appeal No. 1998-2767
Application 08/391,541

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ON BRIEF

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Before HAIRSTON, KRASS, and LALL, Administrative Patent Judges.

LALL, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims of 1 and 3 to 26. Claim 2 has been canceled.

The disclosed invention is related to a computer system and method for diagnosing and isolating faults in multiple

card systems. Typically, a processor simply writes a pattern of data to a particular memory location and then reads back the data from that location to verify proper operation. This process is then repeated for different patterns and different memory locations. The invention provides a diagnostic state machine distinct from the central processor unit. To isolate a fault between a computer system and an external device connected to the computer via an external bus, the computer system simulates a direct memory access (DMA) by the external device without actually employing the external device. To accomplish this, the computer system stores self-generated data and address signals from a back connector that would otherwise connect to the external device. The method of the invention is performed by writing a first value to a first address space defined by addresses on a bus, latching the first value in a first register with a diagnostic state machine, writing the first value from the first register to a second address within the second address space defined by addresses on the bus, reading a second value from the memory over the bus, at the second address, and comparing the second

value to the first value to indicate an error if they are different. The invention is further illustrated by the following claim.

1. In a computer sytem comprising a bus, a processor coupled to the bus, a transceiver, containing a first register and a second register, coupled to the bus, a diagnostic state machine coupled to the bus and associated with a first address space defined by addresses on the bus, and a memory coupled to the bus and associated with a second address space defined by addresses on the bus, the second address space being related to the first address space such that locations in the first address space correspond with locations in the second address space, a method for diagnosing and isolating faults in the computer system comprising the steps of:

writing, from the processor onto the bus, a first value to a first address within the first address space;

latching the first value in the first register using the diagnostic state machine;

writing the first value from the first register to a second address within the second address space, the second address being associated with the first address in the first address space;

reading, by the processor, a second value from the memory over the bus, at the second address; and

comparing, by the processor, the second value to the first value to indicate an error if they are different.

The references relied on by the Examiner are:

Mizuta	4,979,144	Dec. 18, 1990
Davis et al. (Davis)	5,239,637	Aug. 24, 1993

Claims 1, 3, 9 to 10, and 17 to 20 stand rejected under 35 U.S.C. § 103 over Davis, while for the rejection of claims 4 to 8, 11 to 16, and 21 to 26, under 35 U.S.C. § 103 the Examiner adds Mizuta.

Reference is made to Appellants' brief and the Examiner's answer for their respective positions.

OPINION

We have considered the record before us, and we will reverse the rejection of claims 1 and 3 to 26.

In rejecting a claim under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467
(1966), and to provide a reason why one having ordinary skill

in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. System., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings

by the Examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

Furthermore, the Federal Circuit states that "[the] mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification

obvious unless the prior art suggested the desirability of the modification." In re Fitch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), citing In re Gordon, 773 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." Para-Ordnance Mfg. V. SGS Importers Int'l, 73 F.3d 1085, 1087, 37 USPQ 2d 1237, 1239 (Fed. Cir. 1995), citing W. Lish. Gore & Assocs., v. Garlock, Inc., 721 F.2d 1551, 1553, 220 USPQ 311, 312-13 (Fed. Cir. 1983).

Analysis

There are two independent method claims (1 and 15) and two independent apparatus claims (17 and 25). We take claim 1 as an exemplary claim. After reviewing the position of the Examiner [answer, pages 4 to 6 and 8 to 10] and the Appellants' position [brief, pages 9 to 13], we are of the view that the Examiner has not specifically shown the claimed "diagnostic state machine coupled to the bus and associated with a first address space defined by addresses on the bus," and the step of "latching the first value in the first

register using the diagnostic state machine." The Examiner states that "[n]ot particularly taught by Davis is that his system is a diagnostic state machine" [answer, page 5], but asserts that "one of ordinary skill would have wanted to modify Davis to consider one of his processors as a state machine or (emphasis added) to include a diagnostic state machine thereby improving the detection of faults in one's data. ... also, said management function can of itself be considered a diagnostic function" [id.]. Thus, the Examiner has proposed three alternatives for obviousness, i.e., one of the host processors of Davis may be considered as the claimed state machine, or introduce an additional state machine (the Examiner does not explain how and from where) to Davis's system, or merely consider the management function of Davis as a diagnostic function (we assume that the Examiner is here referring to the function of comparing of data at various shadow sites and overwriting the incorrect data with the correct data). In our view, none of these alternatives is any thing more than an over reach by the Examiner to meet the claimed limitations. Even if a state machine were somehow

present in the Davis system, the Examiner has not specifically shown the claimed step of "latching the first value in the first register using the diagnostic state machine." Therefore, we do not sustain the obviousness rejection of claim 1 over Davis.

Independent claim 17 is also rejected as being obvious over Davis. We find that claim 17 contains the limitations discussed above regarding claim 1. Therefore, for the same rationale, we do not sustain the obviousness rejection of claim 17 over Davis.

We next consider the rejection of independent claims 15 and 25 over Davis and Mizuta. Each of claims 15 and 25 contains, inter alia, limitations corresponding to those recited above regarding claim 1. Mizuta does not cure the deficiencies of Davis in meeting those limitations. Therefore, we do not sustain the obviousness rejection of claims 15 and 25 over Davis and Mizuta.

Regarding the dependent claims 3, 9 to 10, and 18 to 20, their obviousness rejection over Davis is not sustained for the same reasons as claim 1.

With respect to dependent claims 4 to 8, 11 to 14, 16 and 21 to 24, and 26, their obviousness rejection over Davis and Mizuta is not sustained for the same rationale as claims 15 and 25.

In conclusion, the Examiner's decision rejecting claims 1 and 3 to 26 under 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)	
ERROL A. KRASS Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
PARSHOTAM S. LALL Administrative Patent Judge	)	

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